I claim:

1. A reader of an RFID system comprising:

excitation circuitry for generating a higher voltage excitation signal;

receiving circuitry for reading a lower voltage transponder signal;

an antenna coupled with said excitation circuitry for transmitting said excitation signal and coupled with said receiving circuitry for receiving said transponder signal; and

a low voltage signal stripping circuit included in said receiving circuitry coupled with said antenna for isolating said transponder signal from said excitation signal preliminary to said receiving circuitry reading said transponder signal, said low voltage signal stripping circuit comprising an inlet resistor, an amplifier, a feedback circuit and a DC shift voltage or a DC shift current source.

2. The reader of claim 1, wherein said inlet resistor is positioned in series between said antenna and said amplifier.

3. The reader of claim 1, wherein said feedback circuit has a pathway including a pair of clamping diodes aligned in series.

4. The reader of claim 1, wherein said feedback circuit has a pathway including a feedback resistor having a resistance.

5. The reader of claim 4, wherein said inlet resistor has a resistance about equal to said resistance of said feedback resistor.

6. The reader of claim 1, wherein said feedback circuit has a first pathway including a first pair of clamping diodes aligned in series in a first direction, a second pathway including a second pair of clamping diodes aligned in series in a second direction opposite said first direction, and a third pathway including a feedback resistor.

7. The reader of claim 1, wherein said inlet resistor is a high voltage component and said amplifier and said feedback circuit are low voltage components.

8. The reader of claim 1, wherein said amplifier and said feedback circuit are included in an application specific integrated circuit.

9. The reader of claim 1, further comprising a summing node positioned upstream of said amplifier and downstream of said inlet resistor, said feedback circuit

and said DC shift voltage or said DC shift current source to sum outputs from said inlet resistor, said feedback circuit and said DC shift voltage or said DC shift current source.

10. The reader of claim 1, wherein said amplifier has a first input coupled with said inlet resistor and a second input tied to a reference voltage.

11. The reader of claim 10, wherein said first input of said amplifier is an inverting negative input.

12. The reader of claim 10, wherein said second input of said amplifier is a non-inverting positive input.

13. The reader of claim 9, wherein said amplifier has a first input coupled with said summing node and a second input tied to a reference voltage.

14. The reader of claim 13, wherein said first input of said amplifier is an inverting negative input.

15. The reader of claim 13, wherein said second input of said amplifier is a non-inverting positive input.

16. A low voltage signal stripping circuit for a reader of an RFID system, said low voltage signal stripping circuit comprising:

an inlet resistor;

an amplifier;

a feedback circuit; and

a DC shift voltage or a DC shift current source.

17. The low voltage signal stripping circuit of claim 16, wherein said feedback circuit has a pathway including a pair of clamping diodes aligned in series.

18. The low voltage signal stripping circuit of claim 16, wherein said feedback circuit has a pathway including a feedback resistor having a resistance.

19. The low voltage signal stripping circuit of claim 18, wherein said inlet resistor has a resistance about equal to said resistance of said feedback resistor.

20. The low voltage signal stripping circuit of claim 16, wherein said feedback circuit has a first pathway including a first pair of clamping diodes aligned in series in a first direction, a second pathway including a second pair of clamping diodes aligned in series in a second direction opposite said first direction, and a third pathway

including a feedback resistor.

21. The low voltage signal stripping circuit of claim 16, wherein said inlet resistor is a high voltage component and said amplifier and said feedback circuit are low voltage components.

22. The low voltage signal stripping circuit of claim 16, wherein said amplifier and said feedback circuit are included in an application specific integrated circuit.

23. The low voltage signal stripping circuit of claim 16, further comprising a summing node positioned upstream of said amplifier and downstream of said inlet resistor, said feedback circuit and said DC shift voltage or said DC shift current source to sum outputs from said inlet resistor, said feedback circuit and said DC shift voltage or said DC shift current source.

24. The low voltage signal stripping circuit of claim 16, wherein said amplifier has a first input coupled with said inlet resistor and a second input tied to a reference voltage.

25. The low voltage signal stripping circuit of claim 24, wherein said first input of said amplifier is an inverting negative input.

26. The low voltage signal stripping circuit of claim 24, wherein said second input of said amplifier is a non-inverting positive input.

27. The low voltage signal stripping circuit of claim 23, wherein said amplifier has a first input coupled with said summing node and a second input tied to a reference voltage.

28. The low voltage signal stripping circuit of claim 27, wherein said first input of said amplifier is an inverting negative input.

29. The low voltage signal stripping circuit of claim 27, wherein said second input of said amplifier is a non-inverting positive input.

30. A low voltage signal stripping circuit for a reader of an RFID system, said low voltage signal stripping circuit comprising:

means for creating a low voltage output signal from a high voltage antenna signal input to said low voltage signal stripping circuit;

means for creating a DC shift voltage or a DC shift current;

means for selectively distributing a feedback signal from an amplifier having an output operating range;

means for creating a summed signal by summing said low voltage output signal, said selectively distributed feedback signal, and said DC shift voltage or said DC shift current; and

means for inputting said summed signal to an amplifier input of said amplifier.

31. The low voltage signal stripping circuit of claim 30 further comprising means for creating a reference voltage.

32. The low voltage signal stripping circuit of claim 31, wherein said amplifier input is a first amplifier input, said low voltage signal stripping circuit further comprising means for creating a reference voltage, a second amplifier input and means for inputting said reference voltage to said second amplifier input.

33. The low voltage signal stripping circuit of claim 30, wherein said low voltage output signal has a low voltage value below an upper voltage limit of said output operating range and said high voltage antenna signal has a high voltage value above said upper voltage limit of said output operating range.

34. A method for processing a high voltage antenna signal waveform comprising the steps of:

providing a high voltage antenna signal waveform including a low voltage transponder signal containing readable information superposed on a high voltage excitation signal;

specifying a location on said waveform where a waveform portion is to be isolated;

specifying a size of said waveform portion to be isolated at said specified location on said waveform;

isolating said waveform portion, wherein said waveform portion contains said readable information; and

reading said readable information on said waveform portion.

35. The method of claim 34, wherein said location is specified by specifying a relative voltage value on said waveform.

36. The method of claim 34, wherein said size of said waveform portion is specified by specifying an absolute voltage range applied to said waveform at said specified location.

37. A method for processing a high voltage antenna signal comprising the steps of:

receiving a high voltage antenna signal containing readable information from an antenna at an input of a low voltage stripping circuit;

limiting a voltage of said high voltage antenna signal to create a low voltage output signal containing said readable information;

creating a DC shift voltage or a DC shift current;

selectively distributing a feedback signal from an amplifier having an output operating range;

creating a summed signal containing said readable information by summing said low voltage output signal, said selectively distributed feedback signal, and said DC shift voltage or said DC shift current;

passing said summed signal through said amplifier to create an amplifier output signal containing said readable information; and

reading said readable information on said amplifier output signal.

38. The method of claim 37, wherein said amplifier provides a gain to said summed signal in response to said selectively distributed feedback signal to create said amplifier output signal.

39. The method of claim 37, wherein said high voltage antenna signal has a voltage exceeding an upper voltage tolerance of said amplifier.

40. The method of claim 37, wherein said low voltage output signal has a voltage below an upper voltage tolerance of said amplifier.

41. The method of claim 37, wherein said voltage of said high voltage antenna signal is limited by passing said high voltage antenna signal through an inlet resistor.

42. The method of claim 37, wherein said amplifier has a first input and a second input held to essentially a same voltage value, wherein said summed signal is

input to said first input and a voltage reference is input to said second input.

43. The method of claim 37, wherein said amplifier has an inverting input and a non-inverting input held to essentially a same voltage value, wherein said summed signal is input to said inverting input and a voltage reference is input to said non-inverting input.

44. The method of claim 37, wherein said feedback signal is selectively distributed by a feedback circuit having a first pathway with a low impedance to said feedback signal when a voltage of said feedback signal is above an upper limit of a predetermined voltage range, a second pathway with a low impedance to said feedback signal when said voltage of said feedback signal is below a lower limit of said predetermined voltage range, and a third pathway with a low impedance to said feedback signal when a voltage of said feedback signal is within said predetermined voltage range.

45. The method of claim 37, wherein said amplifier provides gain to said summed signal varying as a function of a voltage of said feedback signal distributed to said summed signal, said gain being reduced when said voltage of said feedback signal distributed to said summed signal is outside said predetermined voltage range.